What is claimed is:

1. An arithmetic operation method for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising:

first arithmetic operation processing in which a first arithmetic operation is performed on said data by a specified number of bits using a first generative polynomial;

second arithmetic operation processing in which a second arithmetic operation is performed on said data by a specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and

third arithmetic operation processing in which a third arithmetic operation is performed on said data of a specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic operation and second arithmetic operation.

2. The arithmetic operation method for the cyclic redundancy check according to Claim 1, wherein, in said third arithmetic operation processing, said third arithmetic operation is performed by handling said data of said specified number of bits as low-order bits and by handling at least one piece of said

third arithmetic operation result as high-order bits.

3. An arithmetic operation method for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising:

first arithmetic operation processing in which a first arithmetic operation is performed on said data by 32 bits using a thirty-second order generative polynomial;

second arithmetic operation processing in which a second arithmetic operation is performed on said data by 32 bits using a sixteenth order generative polynomial; and

third arithmetic operation processing in which a third arithmetic operation is performed on said data of 32 bits and on the first arithmetic operation result of 32 bits being obtained at a midpoint in said first arithmetic operation processing using said sixteenth order generative polynomial.

4. The arithmetic operation method for the cyclic redundancy check according to Claim 3, wherein, in said third arithmetic operation processing, said third arithmetic operation is performed by 64 bits in total by handling said data of 32 bits as low-order bits and said arithmetic operation result of 32 bits as high-order bits.

5. An arithmetic operation method for a cyclic redundancy

check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation method comprising:

first arithmetic operation processing in which a first arithmetic operation is performed on said data by 32 bits using a sixteenth order generative polynomial;

second arithmetic operation processing in which a second arithmetic operation is performed on said data by 32 bits using said sixteenth order generative polynomial;

third arithmetic operation processing in which a third arithmetic operation is performed on said data of 32 bits and on a first arithmetic operation result of 16 bits being obtained at a midpoint in said first arithmetic operation processing using said sixteenth order generative polynomial;

fourth arithmetic operation processing in which a fourth arithmetic operation is performed on said data by 32 bits using said sixteenth order generative polynomial; and

fifth arithmetic operation processing in which a fifth arithmetic operation is performed on said data of 32 bits, said first arithmetic operation result of 16 bits, and a second arithmetic operation result of 16 bits being obtained at a midpoint in said second arithmetic operation processing using said sixteenth generative polynomial.

6. The arithmetic operation method for the cyclic redundancy check according to Claim 5, wherein, in said third

arithmetic operation processing, said arithmetic operation is performed by 48 bits in total by handling said data of 32 bits as low-order bits and said first arithmetic operation result of 16 bits as high-order bits and wherein, in said fifth arithmetic operation processing, said fifth arithmetic operation is performed by 64 bits in total by handling said data of 32 bits as low-order bits, said first arithmetic operation result of 16 bits as middle-order bits, and said second arithmetic operation result of 16 bits as high-order bits.

7. An arithmetic operation circuit for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising:

a first arithmetic operation section to perform a first arithmetic operation on said data by a specified number of bits using a first generative polynomial;

a second arithmetic operation section to perform a second arithmetic operation on said data by said specified number of bits using at least one piece of a second generative polynomial being same as or different from said first generative polynomial; and

a third arithmetic operation section to perform a third arithmetic operation on said data of said specified number of bits and on at least one piece of an arithmetic operation result being obtained at a midpoint in either of said first arithmetic operation or said second arithmetic operation, or in both said first arithmetic

operation and said second arithmetic operation using at least one piece of said second generative polynomial.

8. The arithmetic operation circuit for the cyclic redundancy check according to Claim 7, further comprising a data combining section to combine said data of said specified number of bits handled as low-order bits with at least one piece of said arithmetic operation result handled as high-order bits and to feed combined results to said third arithmetic operation section.

9. An arithmetic operation circuit for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising:

a first arithmetic operation section to perform a first arithmetic operation on said data by 32 bits using a thirty-second order generative polynomial;

a second arithmetic operation section to perform a second arithmetic operation on said data by 32 bits using a sixteenth order generative polynomial; and

a third arithmetic operation section to perform a third arithmetic operation on said data of 32 bits and on an arithmetic operation result of 32 bits being obtained at a midpoint in said first arithmetic operation section using said sixteenth order generative polynomial.

10. The arithmetic operation circuit for the cyclic redundancy check according to Claim 9, further comprising a data combining section to combine said data of 32 bits handled as low-order bits with said first arithmetic operation result of 32 bits handled as high-order and to feed combined results to said third arithmetic operation section.

11. An arithmetic operation circuit for a cyclic redundancy check which performs arithmetic operations for error detection on data to be transmitted using a plurality of generative polynomials and is used in a communications system in which transmission of said data is accomplished by adding a result from each of said arithmetic operations to said data, said arithmetic operation circuit comprising:

a first arithmetic operation section to perform a first arithmetic operation on said data by 32 bits using a sixteenth order generative polynomial;

a second arithmetic operation section to perform a second arithmetic operation on said data by 32 bits using said sixteenth order generative polynomial;

a third arithmetic operation section to perform a third arithmetic operation on said data of 32 bits and on a first arithmetic operation result of 16 bits being obtained at a midpoint in said first arithmetic operation section using said sixteenth order generative polynomial;

a fourth arithmetic operation section to perform a fourth arithmetic operation on said data by 32 bits using said sixteenth order generative polynomial; and

a fifth arithmetic operation section to perform a fifth

arithmetic operation on said data of 32 bits, said first arithmetic operation result, and a second arithmetic operation result of 16 bits being obtained at a midpoint in said second arithmetic operation section using said sixteenth order generative polynomial.

12. The arithmetic operation circuit for the cyclic redundancy check according to Claim 11, further comprising:

a first data combining section to combine said data of 32 bits with said first arithmetic operation result and to feed a combined result to said third arithmetic operation section, wherein as said combined result, said data of 32 bits is placed at low-order bits and said first arithmetic operation result is placed at high-order bits, and

a second data combining section to combine together said data of 32 bits, said first arithmetic operation result, and said second arithmetic operation result and to feed a combined result to said fifth arithmetic operation section, wherein as said combined result said data of 32 bits is placed at low-order bits and said first arithmetic operation result is placed at middle-order bits, and said second arithmetic operation result is placed at high-order bits.